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Implementation of Adders using Reversible Logic Gates

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Abstract— *The aim of this paper is to a design of a low power efficient adder circuits using reversible logic gates. In this paper, four digital adders are designed using reversible logic gates. In general adders are the building blocks of arithmetic and logic unit, the design is based on the parameters like delay, power, area and number of gates. The main objective of using reversible logic is to avoid information loss and reduce heat dissipation. A newly designed reversible gate called SSS gate is used to design all four adders. The SSS gate itself will act as a full adder if its third input is made to zero. The required codes for the implementation of Adders are written in Verilog HDL. The circuits are simulated and synthesized in Cadence Virtuoso software. The proposed design is compared with existing one's in terms of delay, number of gates used, power required, and area utilized.*

Keywords— Reversible circuits, SSS Gate, Quantum Cost, Adder circuits.

1. INTRODUCTION

Information loss and energy dissipation are the major problems faced in the present-day technology. The problem can be rectified using reversible logic. The reversible gate consists of equal number of outputs and inputs. It also has one to one correspondence between output and input ports. The operation of the circuit is backwards so that the inputs can be easily retrieved from the outputs. And they can be stopped and go back at any point during the time of computation. The conventional gates like XOR, OR, AND which are used in construction of a digital circuits will not perform reversible operations, this leads to information loss which produces dissipation of heat. The loss of information for every bit, generates heat which is given by formula KT*log2 Joules where K is the Boltzmann's constant and T is the Absolute Temperature. The demand for reversible circuits is more in VLSI design because there is no information loss and it dissipates zero heat. So, it provides low power consumption while designing complex VLSI circuits.

Four adder circuits are designed using Reversible Logic Gates. They are designed using SSS, Feynman and Fredkin gates. The first design is the implementation of four-bit Adder/Subtractor using reversible gates which will generate four-bit Sum and a Carry. For implementing four-bit reversible ripple carry adder, four Feynman gates and four SSS gates are utilized. It can be used as both Adder and Subtractor. The operation mechanism can be done by using XOR gate. The Feynman Gate will act as XOR gate in Reversible Logics.

The second circuit is the design of Carry Skip Adder using reversible logic. The Carry Skip Adder is constructed with SSS gate and Fredkin gate. Three Fredkin gates are used to perform the AND operation to compute propagate signal. Single Fredkin gate is used to compute the AND-OR logic which will generate the carry out signal.

The third design is the implementation of Carry Select Adder using reversible logic gates like SSS gate and Fredkin gates. This is the fastest of all adders available which is used in many applications like processors to compute Arithmetic operations. It performs two addition operations in parallel. Two Four-bit ripple carry adders designed using SSS gate and five modified Fredkin gates are used to generate the Carry and Sum for the four-bit carry select adder.

The fourth design is the implementation of Carry Save Adder using Reversible Logic. Peres gate and SSS gates are used to generate Sum and Carry. In reversible Carry Save Adder, all the full adders blocks are replaced by newly proposed SSS gates. It is arranged in a binary tree structure. The total sum is generated by moving the carry sequence to its left side by one unit.

2. LITERATURE SURVEY

In the year 1973, the scientist C.H. BENNETT describes a computation which is carried in Reversible logic which produce no heat dissipation. Because the amount of energy dissipated in entire block is directly proportional to the number of bits erased during the process of the computation. If the circuit is designed in such a way that there is no information loss then it is called as reversible which is mentioned in [2]. Reversible circuits are designed using reversible logic gates. Reversible gate will produce unique output vector for each set of input vector applied and it is vice versa only.

With the help of quantum primitive gates, a new reversible gate is designed. The designed new gates will have a ability to produce all conventional logical operations like AND, NAND, OR, NOR, XOR, XNOR. The design of the full adder is made by using newly proposed SSS Gate. The newly proposed gate is more efficient than the other full adder circuits constructed by Toffoli, Feynman gates and Peres gate [8].

The scientist Landauer explains that both logical irreversibility and physical irreversibility are closely associated and they require a minimum heat generation for every cycle performed. For each bit of information lost produces k*T*log2 Joules of energy, where k is Boltzmann's constant and T the absolute temperature where the operations are being performed. To perform some computations in conventional system some millions of transistors are used. Author [1] proves that there will be no dissipation of heat if blocks are replaced with reversible circuits.

B. Raghu Kanthetal explains the advantages of using reversible logic gates in the implementation of circuits. It decreases garbage outputs, number of gates utilized. Author realized the addition and subtraction operations using DKG gate. The results are compared with circuits which are made with conventional gates. The newly proposed adder/subtractor circuit can be applied vastly in the design of the nanotechnology [4] which has wide applications.

T. Himanshu described that the reversible logic has emerged as a promising technology have applications in quantum computation. The gates such as AND, OR and EX-OR will not work as reversible gates. This work [3] is done by a newly proposed reversible gate called “SSS”. This gate is useful in manufacturing faster and powerful adder circuits.

Yedukondala Rao, explained the reversible TSG gate, Fredkin gate, Toffoli gate used to design the four-bit carry select adder. Proposed design of Carry Select Adder that will compare the power dissipation with the existing work. They presented the design of Carry Select adder using TSG module and Fredkin module. The quantum cost of the circuit is clearly explained in [7].

Ripple carry adder is one of the efficient adders which is easy to design and also easy to analyze but slow in processing. In order to achieve much more speed using carry look a-head adder is advisable but major drawback of this is consumes more area [6]. By keeping these two major drawbacks, carry select adder is advisable.

In carry save adder is designed with HNG and Peres gate. The HNG is used in place of full adder and Peres gate is used on behalf of half adder. These stages are arranged in a binary tree structure to generate a sum and carry [9].

Ashima Malhotra, designed reversible multiplexers which has less quantum cost and less area when compared with conventional one. It is constructed with the help of operation in the Fredkin gate. Later the operation in the Fredkin gate is modified will even decreases the complexity in circuit design [5].

In this report, we are designed a carry skip adder which is having a low energy consumption of higher speed compared with the existing circuit. The structures which are implemented can be accessed by comparing their parameters of speed, power, and energy with the existing adders using cadence software. It has less power and delay, where the values are closer for carry-look ahead adder. It also helps to improves speed and energy dissipation of the circuit [10].

3. REVERSIBLE LOGIC GATES

A. Definitions

3.1 *Quantum cost*

The quantum cost of the circuit is defined as the total number of gates used to realize the given function.

3.2 *Reversible Gate*

A reversible gate has same number of inputs and outputs. It also has one to one correspondence between output and input ports. The aim of the reversible circuits is to decrease the number of gates, delay, garbage outputs, quantum cost.

3.3 *Garbage outputs*

In general, the garbage outputs are of no use for additional computations. Garbage outputs are generated to achieve reversibility nature. Through garbage outputs we can easily retrieve the inputs from the outputs.

3.4 *Reversible functionality*

In Boolean logics, the gates are of irreversible nature. To obtain reversibility the numbers of inputs and outputs should be equal. Here the circuit works on both forward and backward operations.

3.5 *Gate count*

Gate count is the evaluation of number of transistors used to design the circuit.

3.6 *Delay*

Delay of the circuit is defined as the number of gates used in the circuit which are used in the operation.

B. Reversible Logic Gates

1. Feynman Gate (FG)

Feynman Gate is a two input, two output reversible gate denoted by FG. It is shown in the figure 1. The two inputs are A and B. Also, the 2 outputs are shown by P and Q. The outputs are defined as: P=A, Q=A⊕B. For Feynman gate, the quantum cost is 1.

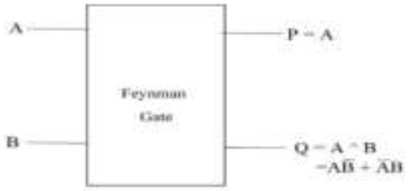
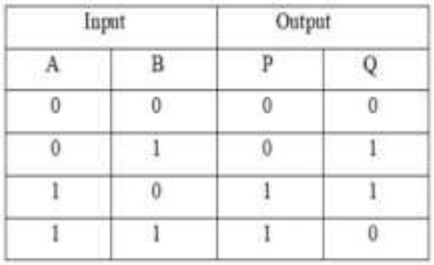


Fig 1: Feynman Gate

The truth table of Feynman Gate is given in table 1 which is shown below

Table 1: Truth table for Feynman Gate



Input		Output	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

FG is used as a copy gate. In the first output port P, the copy of the original signal A will be transmitted. Fan-out is not allowed for reversible logic gates. Feynman gate can be used as EX-OR gate. This output will come at output port i.e. B.

2. Peres Gate

Peres gate is a 3 input 3 output gate denoted by PG. It is shown in figure 2. The inputs to the Peres gate are assumed as A, B and C whereas the outputs are taken by P, Q and R. The outputs are defined as: P= A, Q = A⊕B and R=A.B⊕C. For Peres gate, the quantum cost is four. Peres gate is used in the design of adder circuits because of its low quantum cost.

Peres gate can be used instead of AND gate. When C=0, the Peres gate outputs will be changed as: P=A, Q=A⊕B and R=A.B. Here, AND gate operation will be obtained at R port.

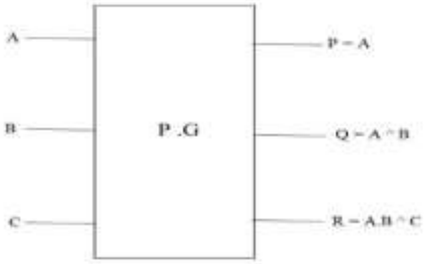
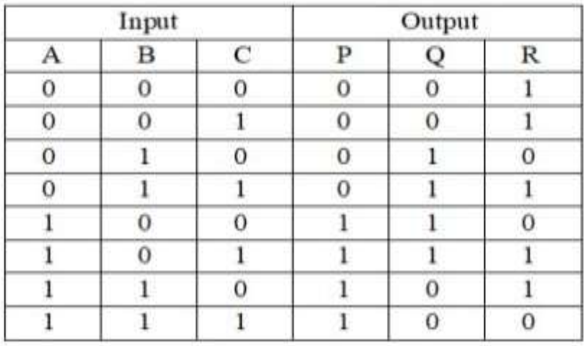


Fig 2: Peres Gate

The truth table of Peres gate is given in table 2 is shown below

Table 2: Truth table for Peres Gate



Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	1
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

3. Fredkin gate

Fredkin Gate is a 3 input 3 output gate. It is shown in figure 3. The inputs are represented by A, B and C whereas the outputs are represented by using P, Q and R. The outputs are defined as: P=A, Q=A′.B⊕A.C and R=A′.C⊕A.B. For Fredkin gate, the quantum cost is 5.

Fredkin gate will act as multiplexer. In Fredkin gate the select line will be A and the inputs for mux are B and C. Depending on the value of A, either B or C will come as output. It can be also used as AND gate. When C=0, the output port R will be changed to A.B.

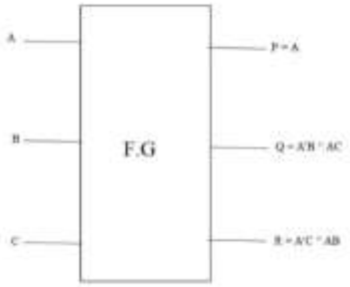


Fig 3: Fredkin Gate

The truth table of Fredkin gate is given below

Table 3: Truth table for Fredkin Gate

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

4. SSS gate

SSS gate is a 4 input and 4 output reversible gate. It is shown in figure 4. The inputs are represented by A, B, C and D whereas the outputs are represented by P, Q, R and S. The outputs are defined as: P=A, Q=A⊕B⊕D, R=A⊕B and S=(A⊕B)D⊕(A.B⊕C). This single gate can be replaced by full adder circuit.

When C=0, SSS gate will produce the sum and carry signals. The inputs should be applied at A, B and D. The sum and carry will be obtained at Q and S ports respectively. The inputs are A, B and C_{in}. The sum and carry expressions are given as Q=A⊕B⊕Cin, S=(A⊕B)C_{in}⊕(A.B).

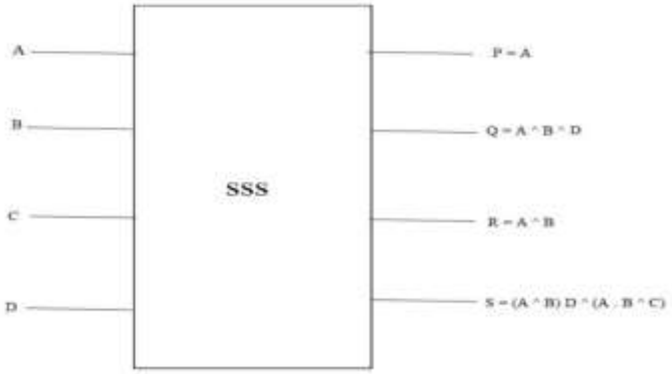
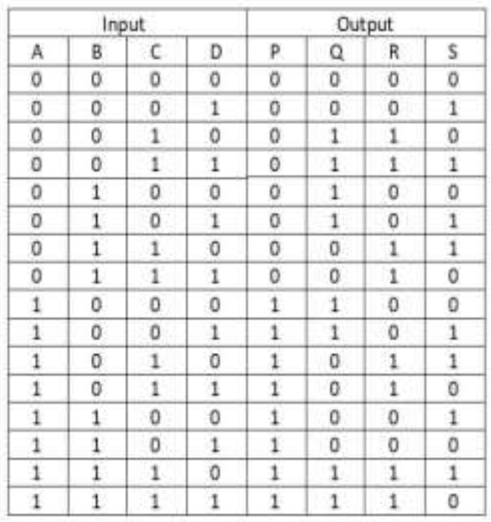


Fig 4: SSS Gate

The truth table of SSS gate is given below

Table 4: Truth table for SSS Gate



Input				Output			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	1	1	0
0	0	1	1	0	1	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	0	1	1
0	1	1	1	0	0	1	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	0	1	1
1	0	1	1	1	0	1	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	0	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	0

4. PROPOSED DESIGN

4.1 ADDER/SUBTRACTOR

First, we have designed a ripple carry adder using a reversible gate called SSS gate. This is a four-input and four-output gate. The operation of the circuit is based on the inputs we have given. This gate itself will act as a full adder by making the 3rd input zero. The sum is generated at the second output and the carry is generated at the fourth output. If we use the inputs as A=A, B=B, C=0, D=C_{in} then the expressions for both sum and carry will be given as

$$\text{Sum}(Q) = A\oplus B\oplus D$$

$$\text{Carry}(S) = \text{Cin}(A\oplus B) \oplus A.B$$

Now a reversible gate called Feynman is used which acts as XOR. So, with the help of XOR and the ripple carry adder we have designed a circuit called Adder/Subtractor.

For adder: $A+B$

For subtractor: $A+(-B) = A - B$.

The operation of the circuit is based on the input given to the XOR gate. For EX-OR gate if one of the inputs is 0 then the expression will be $B\oplus 0$. The equivalent value will be B. Similarly, if one of the inputs is 1 for EX-OR gate then the expression will be $B\oplus 1$. The equivalent value will be B’.

$$B\oplus 0=B$$
$$B\oplus 1=B'$$

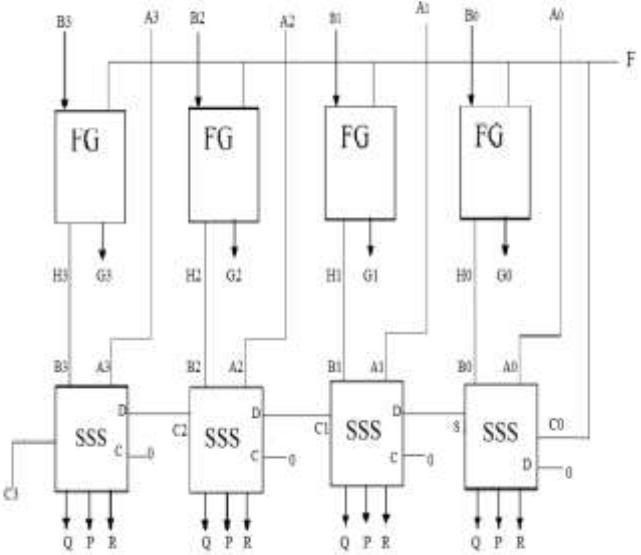


Fig 5: Adder/ Subtractor

Here the circuit operation depends on the control input F. one input vector (An) is directly given to first input of the SSS gate. The second input vector (B_n) is given to Feynman gate which acts as an XOR in reversible logic. The output of the Feynman gate will be given as the second input for SSS gate. The third input vector for the SSS gate will be taken from the previous state carry of the SSS gate. The outputs P and R are the Garbage outputs. The final carry will be obtained from the S_4 output of the SSS gate. The sum/Difference outputs will be obtained at Q_0, Q_1, Q_2, Q_3 outputs of the SSS gate.

The combination of four SSS gates will gives the ripple carry adder. In the adder/subtractor circuit one ripple carry adder is used.

4.2 CARRY SKIP ADDER

In the Carry Skip Adder four SSS gates and four Fredkin gates are used. The combination of four SSS gates will act as a Ripple Carry Adder. The purpose of the Fredkin gate(F_4) is to perform Multiplexer operation. The remaining gates Fredkin gates F_1, F_2 and F_3 will perform AND operation if the third input of the Fredkin gate is made to '0'.

The R0, R1 outputs of SSS_1 and SSS_2 are fed to Fredkin gate(F_2) as inputs. The third input for F_2 gate is '0'. The output for the F_2 gate will be $R_0.R_1$. Similarly, for the SSS_3 and SSS_4 gate outputs R_2 and R_3 will be given to F1 gate as inputs. The output of F_1 gate will be $R_2.R_3$. the outputs of F_1 and F_2 gates will be fed as input to F_3 gate. Here the F_3 gate will perform AND operation this will generate the propagate signal for carry skip adder. Finally, the generated propagate signal is given as input to F_4 gate which acts as a select line to the Fredkin gate (MUX). The final carry is given as input to F_4 (MUX). the other input is initial carry (C_{in}=0) for MUX. Based on the value of the select line the final carry will be generated and is fed to further stages.

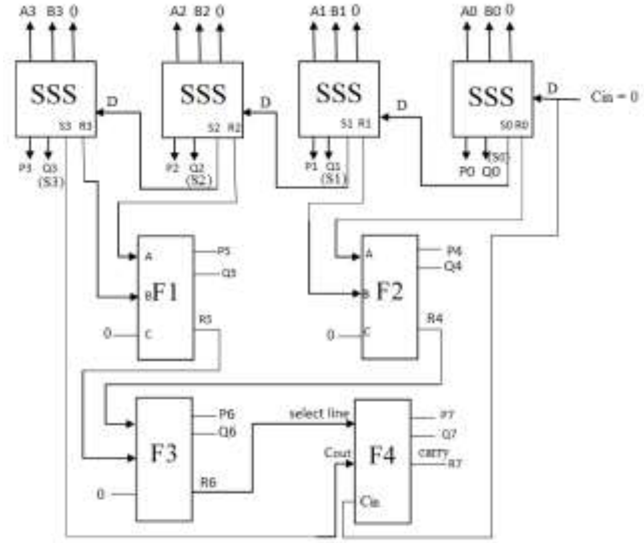


Fig 6: Carry Skip Adder

4.3 CARRY SELECT ADDER

The third design is a carry select adder using reversible gates. In this paper, a carry select adder is designed using 8 SSS gates and 5 modified Fredkin gates. Here 2 ripple carry adders can be used or 8 SSS gates to perform addition operation.

The sum and carry will be calculated in one ripple carry adder when the initial SSS gate inputs are made to a=A b=B c=0 and D= C_{in}=1. The sum will be generated at Q vector of the ripple carry adder. The carry output will be generated at S vector. The carry will be further cascaded further. The final carry will be given to the mux.

The sum and carry will be calculated for another ripple carry adder when initial SSS gate inputs are made to a=A, b=B, c=0, d=c_{in}=1. The sum is generated at Q vector of the ripple carry adder. The individual carry output will be given to final input for the next stage gates. The final carry is generated and given to the multiplexer.

The modified Fredkin gates(F_1) will have low quantum cost when compared to the Fredkin gate. The C_{in} will be made to zero. and R_4 and R_0 will be the inputs for the modified Fredkin gate. These are the sum(S_0) outputs of the ripple carry adders. The output will be obtained at the third port(R_8).

The inputs of the modified Fredkin gate will be R_5, R_1 and P_8. The output will be at R_9. This is the sum(S_1) output of the ripple carry adder.

The inputs for the modified Fredkin gates will be R_6, R_2 and P_9. This P_9 will come from the previous stage output of the Fredkin gate. The output of the gate will be R_{10}. The sum (S_2) will be present at R_{10}.

Similarly, the inputs for the final Fredkin gate will be R_7&, R_3 and P_{10}. This P_{10} will be the output of the previous stage output of the Fredkin gate. The sum(S_3) will be obtained at the R_{11} port of the gate.

To calculate the carry out we use another Fredkin gate which actually works as multiplexer. The S_3, S_7 and P_{11} are the inputs. The outputs will be P_{12}, Q_{12} and R_{12}. This R_{12} is the carry output of the carry select adder.

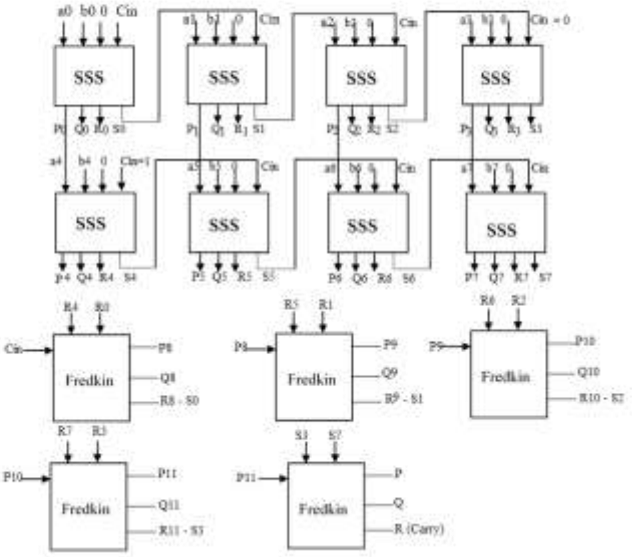


Fig 7: Carry Select Adder

4.4 CARRY SAVE ADDER

The fourth design is a carry save adder using reversible Peres Gate and SSS Gate. Here 1 ripple carry adder is used to perform operation.

Initially the input vectors A_0 and B_0 are given to SSS gate(S_1) where C=0 and D=Cin. The inputs A_1 and B_1 are given to Peres Gate(P_1) where third input is zero. the inputs A_2 and B_2 are given to Peres gate(P_2) by making the third input to zero. Finally, the input vectors A_3 and B_3 are given to Peres Gate(P_3) by making the third input zero.

The carry generated by SSS gate(S_1) is given as the first input to Peres Gate(P_4). Here the Peres Gate(P_1) performs EX-OR operation and generated output of P1 gate is given to Peres gate(P_4). The third output of the P_4 is given to S_2.

The third output of P_1 is given to S_2. The second output of the P_2 is given to S_2. By making the third input to zero. the carry generated by S_2 is given as the input to S_3.

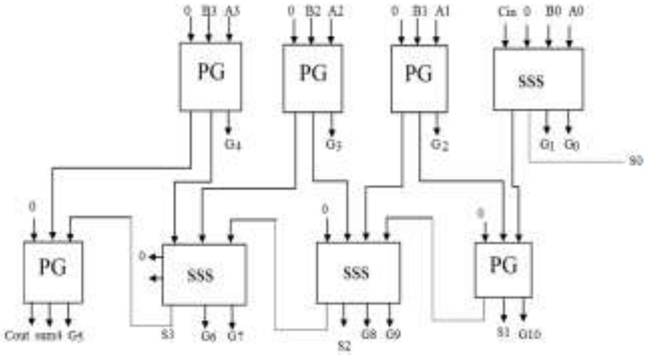


Fig 8: Carry Save Adder

The third output generated by P_2 is given to S_3. The second output of P_3 is given as the input to S_3. Finally, the carry generated by S_3 and the third output generated by P_3 is given as input to Peres Gate (P_5). Here the carryout will be produced at the output of the Peres Gate(P_5)

5. Results and Discussions

The parameters like area, power and delay for the four adders (Adder/Subtractor, Carry Skip Adder, Carry Select Adder and Carry Save Adder) with and without reversible logics are given in the below Table5 and Table 6.

Table 5: Comparision of parameters for adders using 45-nm technology

Comparision of parameters for adders using 45nm technology						
	Reversible logic			Irreversible logic		
Parameters	Area (units)	Delay (ps)	Power (nW)	Area (units)	Delay (ps)	Power (nW)
save	234.1	984.4	5471.96	698.54	1260.6	16,396.09
skip	325.65	718.4	4880.4	600.08	994.4	7296.94
select	532.48	718.2	8082.33	789.87	1039.2	15425.59
Add/sub	226.6	480.4	3163.74	743.65	951.6	6914.05

Table 6: Comparision of parameters for adders using 180nm technology

Comparision of parameters for adders using 180nm technology						
	Reversible logic			Irreversible logic		
Paramet ers	Area (units)	Delay (ps)	Power (nW)	Area (units)	Delay (ps)	Power (nW)
save	468.27	1482. 2	37,790. 5	1396.8 5	1903. 8	116566.98
skip	663.5	3836	14499.8 0	1,164	4198. 16	33836.64
select	1164.0 4	1076. 1	55494.0 8	1990.5 1	1575. 10	104921.62
Add/sub	465.62	718.5	21713.4	651.86	1438. 5	50427.1

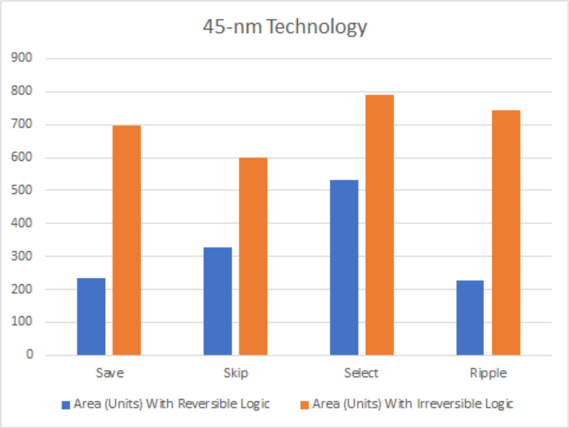


Fig 9: Area Comparison of different adder circuits using 45nm technology

Fig 9 shows the area comparison of different adder circuits using 45-nm technology. In this select area takes high area and ripple carry occupies less area when compared to other adder circuits mentioned in this paper.

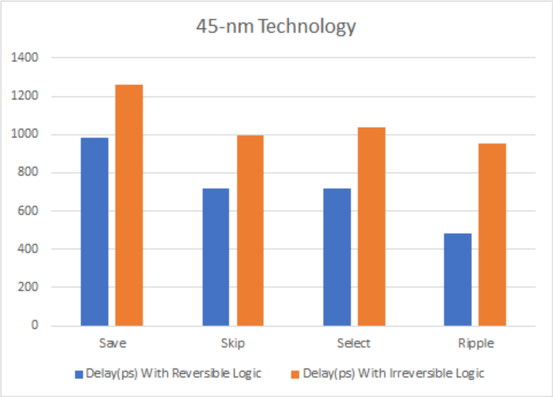


Fig 10: delay Comparison of different adder circuits using 45nm technology

Fig 10 shows the delay taken by the different adder circuits using 45-nm technology. Save adder has highest delay and ripple carry adder has the lowest in terms of delay.

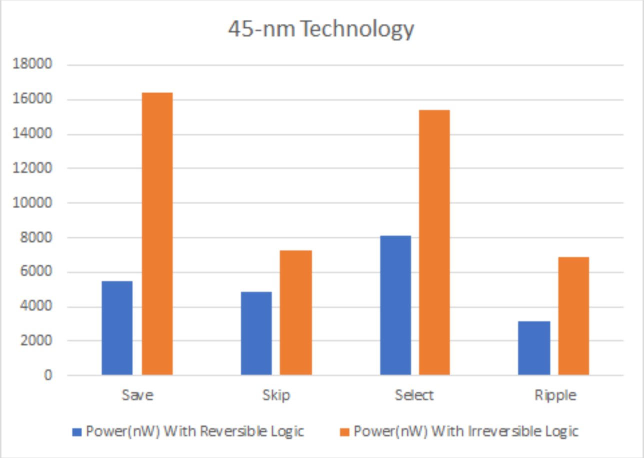


Fig 11: power Comparison of different adder circuits using 45nm technology

Power consumptions for different 4-bit adders circuits are shown in the fig 11. In terms of power, save adder with irreversible adder consumes high power and skip adder has the lowest. Approximately, 70% less power for reversible save adder when compared to irreversible logics.

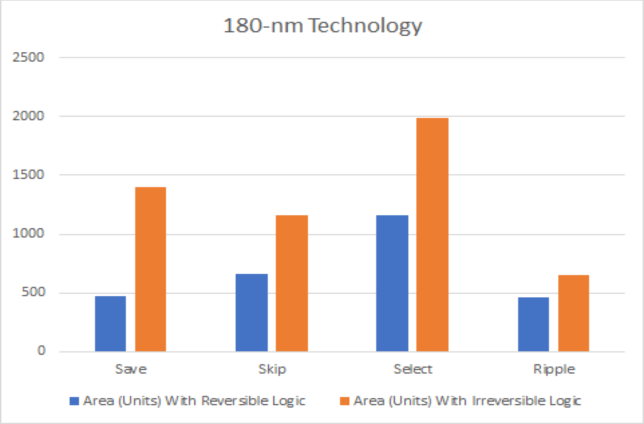


Fig 12: Area Comparison of different adder circuits using 180nm technology

Fig 12 shows the area taken adder circuits by using the 180-nm technology. In terms area, reversible select adder has lesser area (50%) than irreversible logics.

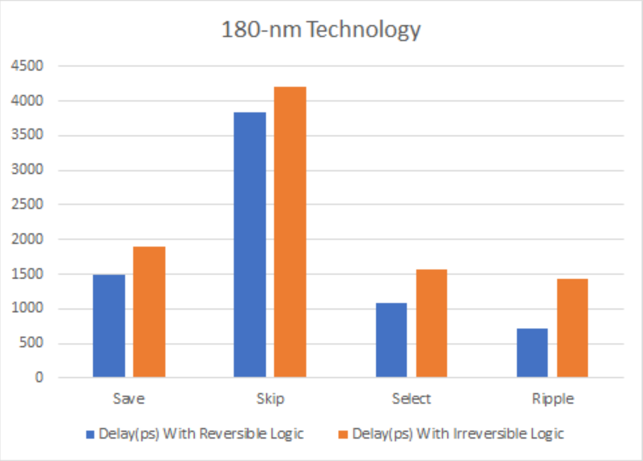


Fig 13: Delay Comparison of different adder circuits using 180nm technology

Fig 13 shows the delay taken by the ports. In the 180-nm technology, Skip adder will have high delay (10%).

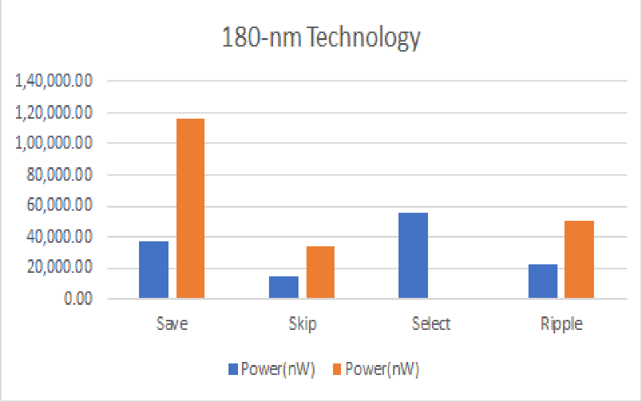


Fig 14: power Comparison of different adder circuits using 180nm technology

In the fig 14 the power consumption for different circuits are compared. The save adder has highest power consumption which is approximately 70%.

The below shown figure 15 demonstrates the design of full adder circuit with 10T technology in cadence virtuoso software.

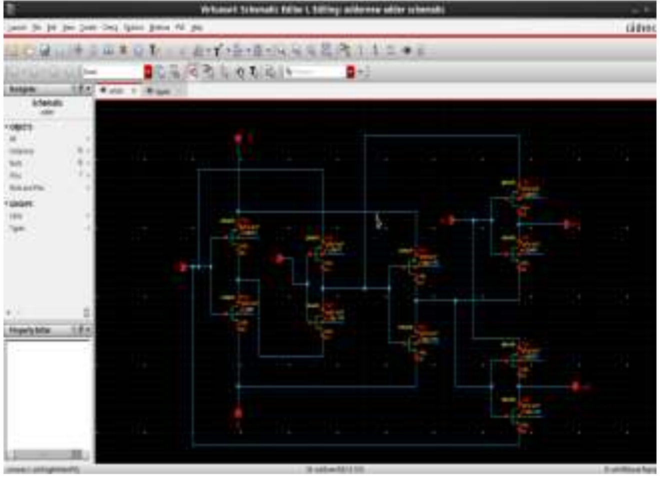


Fig 15: Full adder using 10T technique

Figure 16 explains the ripple carry adder using full adder in cadence virtuoso software.

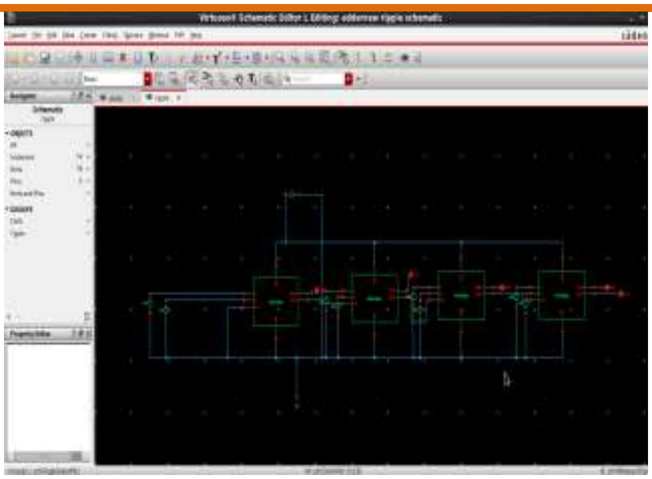


Fig 16: Ripple Carry Adder

6. Conclusion

The proposed 4-bit adders have less area power and delay when compared to irreversible logic circuits. Here the problems like information loss and heat dissipation are avoided. The advantage of 1st circuit is that it acts as both adder and subtractor but the remaining 3 adder circuits have parallel operation which will reduce the computation time.

7. References

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