International Journal of Academic Engineering Research (IJAER)
ISSN: 2643-9085
Vol. 5 Issue 3, March - 2021, Pages: 1-7

Schottky–Barrier Quantum Well In Two-Dimensional Semiconductor Nanotransistors

Jurabek Abdiyev[1], Elyor G'aybulloyev[2], Sherzod Yarashev[2*], Begzod Erkinov[2]

[1]Physical-technical Institute of NPO "Physics – Sun" of Uzbekistan Academy of Sciences Uzbekistan, Tashkent, Chingiz Aitmatov street 2B.

[2]Tashkent University of Information Technologies named after Muhammad al-Khwarizmi, Uzbekistan, Tashkent, Amir Temur street 108.

Corresponding author: sherzodyarashev1997@gmail.com (Sh. Yarashev)

Abstract: *Two-dimensional (2D) semiconductors are promising candidates for quantum-well devices with the inherent quantum confinement of the subnanometer thickness along the out-of-plane direction. Coulomb/quantum oscillation phenomena have been demonstrated in 2D semiconductors devices, including artificial quantum dots with local electrostatic gating and stacked heterostructure quantum wells. However, the exact quantized energy states, let alone the complexity of the device structures and low observation temperature, have not been clearly revealed. Here, we report a rational fabrication platform of 2D semiconduc tor nanotransistors to directly construct a Schottky-barrier quantum well (SB-QW) for quantized energy states engineering. The feature size of the quantum well is tailored by a vertical nanochannel of monolayer transition metal dichalcogenides (TMDCs) via an insulating spacer. Meanwhile, the potential barrier is constructed by the Schottky barrier. Quantum oscillations are clearly observed and the quantized energy states are extracted from the source-drain current modulated with the gate bias. Such quantum oscillations are preserved up to ~100 K with a channel length of approxi-mately 16 nm. With an evaluated Schottky barrier height of approximately 27 meV, the quantized energy states are estimated from 2 to 24 meV near the conduction band edge, consistent with corresponding explicit principal quantum numbers. Our work demonstrates the feasibility of moving 2D van der Waals semiconductor nanotransistors towards quantum transistors.*

Keywords: Schottky-barrier quantum well 2D semiconductor nanotransistors Quantum confinement effect Quantized energy states Quantum oscillations.

1. INTRODUCTION

Two-dimensional (2D) semiconductors have been considered as 2rom2ising candidates to overcome the short channel limit owing to their atomic-scale thickness and the absence of dangling bonds [1,2], compatible with current silicon-based in-plane CMOS fabri-cation technologies [3e5], subsequently to further achieve Moore's law [6e8]. In contrast to three-dimensional semiconductors having channels with finite thicknesses, a van der Waals 2D semi-conductor, particularly in monolayer, provides an ideal criteria for a short channel length, i.e., l_{ch} (3e5) l, where l_{ch} is the channel length and l is the natural length related to the thickness of the channel [9]. Much attention has been paid to the fabrication of short channel transistors of 2D semiconductors in order to achieve high on-current by focusing on the classical regime [10e19]. These fabrication strategies mainly rely on high-resolution electron-beam lithography or are guided by one-dimensional nanogaps or nano-wires. However, along with the complexity and scarce availability of the devices, a tenable platform is still lacking to date. Moreover, when the devices are shrunk to sizes in the nanoscale, approaching the de Broglie wavelength of the carrier, l_{dB} ¼ h/p, where h is the Planck constant and p is the momentum, the quantum effect will manifest in the devices. The primary concern to implement a quantum device is to understand and analyze the quantized energy states, which can further be applied for better design of nanoelectronics.

Quantized energy states have been observed in zero-dimensional nanoparticles [20e23], one-dimensional nanowires and nanotubes [24e26]. 2D semiconductors, with an inherent one-dimensional quantum confinement of the subnanometer thickness along the out-of-plane direction, constructed by the weak van der Waals interaction, provide more chances for quantum engineering. Quantum confinement has been demonstrated with 2D semi-conductors via liquid-exfoliated quantum dots [27,28], post-etching fabricated nanostructures [29,30], gate-defined quantum dots with local electrostatic gating [31e35], and synthetic or stacked heter-ostructure quantum wells [36e39]. However, the feature size of the confinement is considerably large, i.e., over 50 nm (see supplementary Table S1). This limits the observation of the quan-tum phenomena at low temperature with small discrete energy levels. Moreover, a precise analysis of the quantized energy states is still far from being clearly understood.

In this report, we would like to explore a rational fabrication platform and accurately analyze the quantized energy states o f the 2D quantum device. For this purpose, the nanometer-scale 2D semiconductor transistors are directly defined via an ultrashort vertical channel by transferring the molybdenum disulfide (MoS_2) monolayer onto the vertically aligned sourceedrain electrodes, separated by an ultrathin hBN insulating layer. The Schottky bar-riers at the metalesemiconductor junctions induce a quantum well potential, which confines the carriers in the vertical MoS_2 nano-channel. The resonant tunneling of the discrete quantized energy states, which are controllable under the gate bias, has been demonstrated in such Schottky-barrier quantum wells (SB-QW) of 2D Semiconductors. Quantum oscillations and diamond-like pat-terns are clearly observed in the transport characteristics.

2. CONCEPT OF THE SB-QW IN 2D NANOTRANSISTORS

Fig. 1a depicts the schematic of a nanometer-sized 2D semi-conductor channel with a channel length defined by the thickness of the insulating spacer vertically separating the top and bottom electrodes [40], together with the equivalent simplified model of the device (Fig. 1b). Uniquely, the channel structure behaves as a vertical sub-nanometer nanoribbon for 2D semiconductors with the carrier transport perpendicular to the "ribbon" between the source (S) and drain (D) electrodes. Fig. 1c shows the optical image of one typical device with a monolayer MoS_2, synthesized by the chemical vapor deposition (CVD) method (See Figure S1 for more details regarding the device.). The channel length is approximately 16 nm, which is determined by the thickness of the hBN sp acer, as measured using atomic force microscopy (Figure S1). The top and bottom Au electrodes are used to build the Schottky barriers in the AueMoS_2 junctions, forming a one-dimensional quantum well structure confined between the two electrodes. The source-insulating spacer-drain (SID) pattern is prepared after etching the unpassivated part of the hBN spacer using reactive ion etching. Wave-like characteristics of the carrier and quantum effect will become prominent when the size of the 2D semicond uctor channel approaches the de Broglie wavelength of the carrier. Consequently, the discrete energy levels will be explicitly manifested (Fig. 1d). These quantized energy levels can be modulated by a gate bias with the top gate.

3. EXPERIMENTAL SECTION

3.1. SYNTHESIS OF MOS_2 AND WSE_2 BY CVD TECHNOLOGY

The monolayer MoS_2 was synthesized via the two-zone atmo-spheric-pressure chemical vapor deposition (APCVD) method. Ammonium heptamolybdate (AHM, Sigma-Aldrich, 431346) and sulfur powder (S, Sigma-Aldrich, 213292) were used as the corre-sponding molybdenum and sulfur sources, with a growth tem-perature of 750 C [41]. The monolayer WSe_2 was also synthesized via the two-zone APCVD method, with ammonium metatungstate hydrate (AMT, Sigma-Aldrich, 463922) and selenium powder (Se, Sigma-Aldrich, 229865) as the corresponding tungsten and sele-nium sources, with a growth temperature of 750 C [42].

3.2. DEVICE FABRICATION

The nanoscale channel 2D semiconductor transistors were fabricated assisted with mechanical exfoliation, dry transfer, electron beam lithography, metal evaporation, and reactive ion etching.

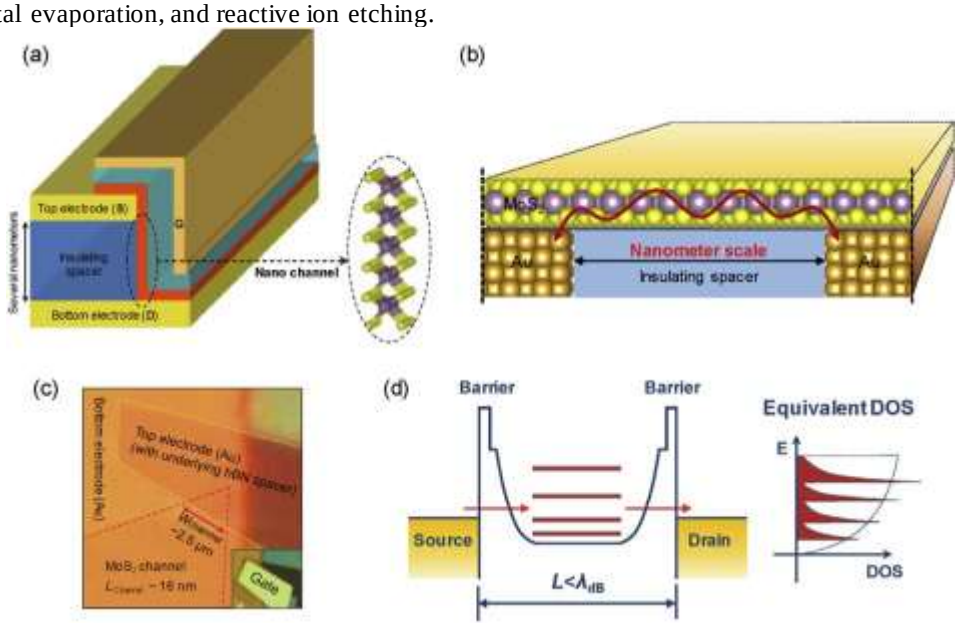

Fig. 1. Schematic illustration of the confined nanoscale-channel 2D transistor between van der Waals-type Schottky barriers. (a) Schematic three-dimensional view of the device layout with five components, i.e., bottom electrode (Au), insulating spacer (hBN), top electrode (Au), vertical type 2D nanochannel (MoS_2), and top-side gate (hBN and Au). (b) Simplified model of the device with wave-like transport behaviour. (c) Optical image of one typical device prior to the gate fabrication. Inset, optical image of the fabricated gate. (d) Schematic band structure of the device with gate modulation (left), and discrete energy levels of the MoS_2 nanochannel due to the quantum confinement effect (right).

The detailed fabrication processes are present in our previous report [40]. Figure S1 also demonstrates the main steps with optical images.

3.3. DEVICE CHARACTERIZATION

The electrical characterization was performed in high vacuum (approximately 10^{6} torr) with the Lake Shore probe system (CRX-VF) and the semiconductor analyzer (Keithley 4200 system). The measurement was performed from the base temperature of the system (less than 15 K) to 300 K.

4. RESULTS AND DISCUSSION.

4.1. QUANTUM OSCILLATIONS IN THE TRANSPORT CHARACTERISTICS

To investigate the transport characteristics of the devices, we performed electrical measurements with the probe system as discussed above. The temperature-dependent transfer curves of the device between the temperatures of 14 K and 300 K are shown in logarithmic and linear scales at a sourceedrain voltage (V_{ds}) of 1 mV (Fig. 2a and b). Regular oscillations of the source-drain current (I_{ds}) are clearly prominent at temperatures of <100 K and gradually weaken at high temperatures. To clearly visualize the oscillation effect, the differential transconductance (G_m ¼ dI_{ds}/dV_g) is plotted in Fig. 2c. Such regular oscillations strongly indicate that resonant tunneling through discrete energy levels occurs in the device. These discrete energy levels are shifted by the gate bias in the I_{ds} char-acterization with V_g. In addition to the oscillation features, the background current increases significantly at higher temperatures. This results from the thermionic emission current through the Schottky barrier. For a quantitative investigation, the temperature-dependent transfer curves are extracted and described using Arrhenius curves via the 2D thermionic emission model (Figure S2). The near-linear relationship between ln ($I_{ds}/T^{3/2}$) and 1000/T is retained in the high temperature range. In contrast, the linear relation deviates at low temperature, indicating that the tunneling mechanism is dominant at a lower temperature. This is also verified by the negligible variation of I_{ds} with the temperature at 14, 25 and 36 K (see Figure S2). The control device with hBN only (prior to transferring the MoS_2 channel) shows current below 1 pA, which is much lower than the current through MoS_2 channel device (in the order of hundreds pA at V_g ¼ 0 V with V_{ds} ¼ 1 mV) (Figure S3). The influence of the leakage current on our oscillation signal is negligible.

Similar oscillation features also manifest in the V_{ds}-dependent GeV_g characteristics (G ¼ I_{ds}/V_{ds}) at 14 K, with low sourceedrain voltages (1 mV and 10 mV), and smear out at high voltages (100 mV and 200 mV) (Fig. 2d). This can be explained by the bias-induced band tilt (Fig. 2d). The band offset is negligible when the sourceedrain bias is low. Electrons tunnel through the Schottky barrier at the junction and resonant tunneling occurs in the MoS_2 channel, which is further modulated by the gate bias. The band is tilted when the sourceedrain bias is high and exceeds the higher energy levels of the MoS_2 channel, subsequently diminishing the quantum oscillations. Such quantum oscillation features with V_{ds} confirm the quantum confinement effect in our devices, and thus, exclude the possibility of noise from measurements. To demon-strate the relevance of the electron channel of MoS_2, we further explored the vertical nanochannel of tungsten diselenide (WSe_2) for hole transport (Fig. 2e and S4). Similar quantum oscillations were observed in the p-type WSe_2, confirming the validity of 2D semiconductors for vertical nanochannel field effect transistor (FET) devices.

Fig. 3a and b shows the varying drain current (I_{ds}) and differ-ential transconductance (G_m) mappings with the temperature and gate bias for the MoS_2 nanochannel device. Discrete peaks are consistently observed till a high temperature of approximately 100 K. Such discrete features at high temperatures are weakened by thermal broadening (Fig. 3c). The thermal broadening width is approximately 9 mV at 100 K, estimated by ~ k_BT, where k_B is the Boltzmann constant. This indicates average energy-level spacing and will be discussed later. Additionally, the thermionic emission current becomes dominant at high temperatures, extinguishing the features of the discrete peaks.

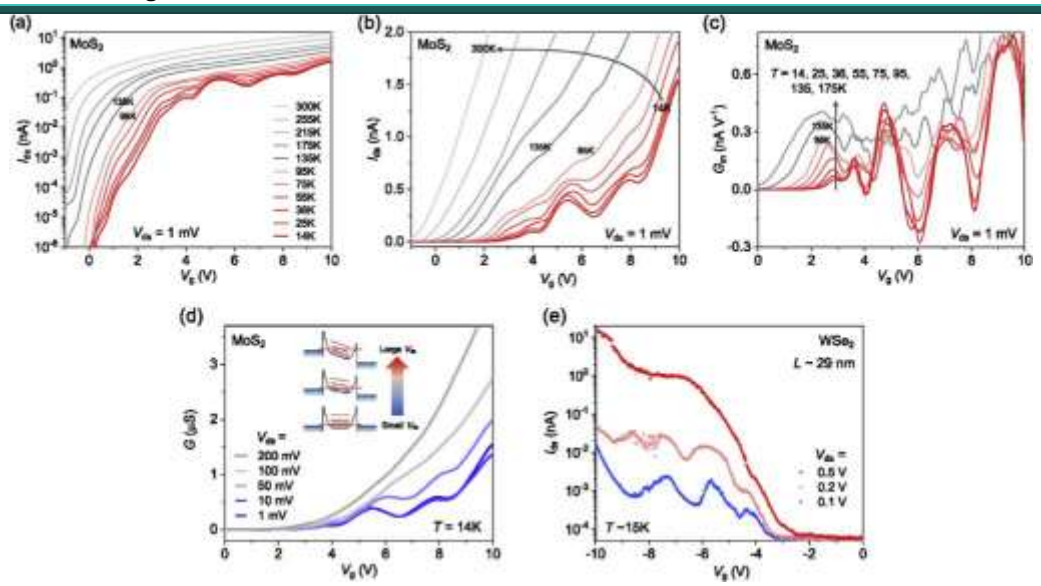

Fig. 2. Quantum oscillations in the transport characterization of the nanoscale-channel 2D transistor. (a) $I_{ds}eV_g$ transfer curves of MoS_2 device in logarithmic scale with V_{ds} of 1 mV at different temperatures from 14 K to 300 K. (b) Linear-scale transfer curves in a. (c) G_meV_g curves extracted from the first derivative of the $I_{ds}eV_g$ curves. Here, G_m is the transconductance. (d) GeV_g curves of the MoS_2 device at T ¼ 14 K with different V_{ds} of 1e200 mV. Inset, V_{ds} effect on the band tilting. Here, G ¼ I_{ds}/V_{ds} is the conductance. (e) Similar oscillations of the hole transport in the WSe_2 vertical nanochannel transistor with a channel length of ~29 nm.

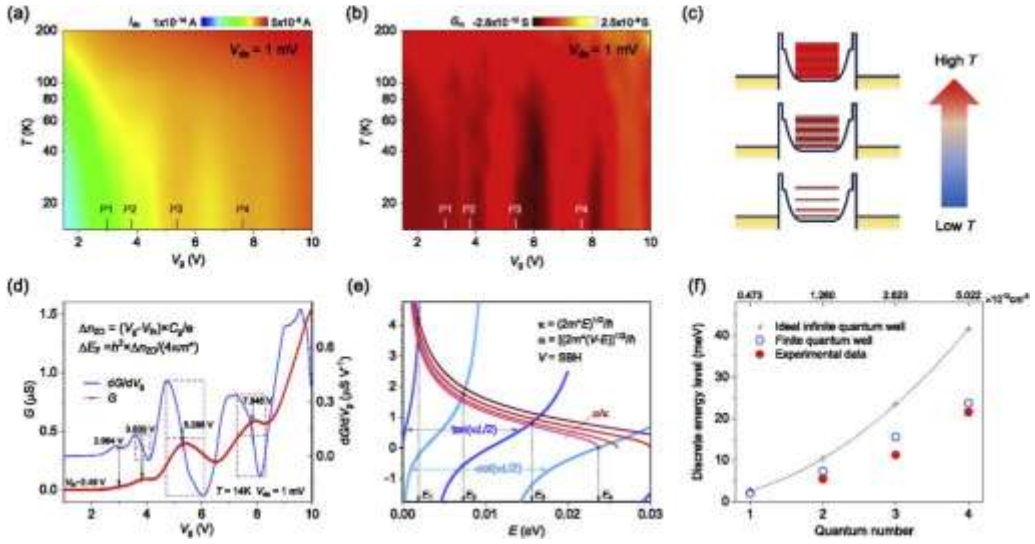

Fig. 3. Discrete peaks and quantized energy levels of MoS_2 nanotransistor. (aeb) Discrete peaks observed in the mapping of I_{ds} (a) and G_m (b) with V_g and T. For better demon-stration, T is set in the logarithmic scale. (c) Schematic illustration of the variation of the band structure with temperature to depict the thermal smearing effect. (d) Estimation of the discrete peak positions for GeV_g and dG/dV_geV_g curves. The variation of the carrier density and Fermi level are calculated with the inset equations. (e) Graphical solution of the finite potential well. Since the Schottky barrier height (SBH) also varies with V_g, four different values of the SBH, corresponding to the oscillation peaks, are considered as the boundary potentials to calculate the discrete energy levels. (f) Comparison between the estimated discrete energy levels from the ideal infinite potential quantum well, finite potential quantum well model, and experimental data.

4.2. VERIFICATION OF THE QUANTUM CONFINEMENT EFFECT

To verify whether the quantum confinement effect can occur in our device, we estimate the de Broglie wavelength (l_{dB}) of MoS_2 [36], which is defined as

$$\lambda_{dB} = \frac{h}{p} = \frac{h}{\sqrt{2m*E_k}} \approx \frac{h}{\sqrt{2m*k_BT}} \qquad (1)$$

where h is the Planck constant, p is the momentum, E_k is the kinetic energy, k_B is the Boltzmann constant, and m* is the effective mass of the electron in MoS_2, which is approximately 0.55e0.57m_e [43,44]. Here we only consider the thermal energy to estimate the de Broglie wavelength. The acceleration effect of the source-drain bias on the carriers is negligible when the applied bias is small (e.g., 1 mV in our measurement). This effect is even much smaller due to inelastic scattering in the channel. The estimated de Broglie wavelength at 100 K is ~17 nm, which is comparable to the channel length of ~16 nm. This explains the possibility for observing the discrete levels up to 100 K. The de Broglie wavelength becomes longer at lower temperatures, significantly revealing the oscillation features in our devices.

We note that the conventional Coulomb blockade, induced by the charging effect, can also generate similar oscillation features [45,46]. To estimate the contribution of the conventional Coulomb blockade effect, we calculate the charging energy due to the gate capacitance. In our device, the classical capacitance between the gate electrode and the channel (C_g) is approximately 6 10^{17} F, with the hBN gate insulator with a thickness of approximately 21 nm. The corresponding charging energy of a single electron (E_c ¼ $e^2/2C_g$) is approximately 1.3 meV, when only the gate-channel capacitance is considered. This estimated value is much smaller in our device when the parasitic capacitance between the gate elec-trode and source/drain electrodes is considered. This capacitance is estimated to be over 100 times larger than the gate capacitance from the geometry of our device. Therefore, we exclude the influ-ence of the conventional Coulomb blockade effect in our device.

Additionally, the quantum oscillations in the transfer curves can also be observed when the charge-trap-induced disorder exists in the channel [47,48], which normally occurs in samples with a high defect density. However, the defect density in our MoS_2 is approximately 4 10^{11} cm^{-2} as measured by the scanning tunneling microscope [49], which is much smaller than the carrier density modulated by the gate bias (~7 10^{12} cm^{-2}). (See Figure S5 in the supplementary material for a more detailed discussion). The ultrasmall hysteresis (Figure S6) also confirms that our devices are quite clean. The disorder model of hopping [47] does not match our transport characteristics (Figure S7).

4.3. ESTIMATION OF THE DISCRETE QUANTIZED ENERGY STATES

In order to calculate the energy level positions in the quantum confined finite quantum well in the MoS_2 nanochannel, we first consider the GeV$_g$ and dG/dV$_g$eV$_g$ curves together (Fig. 3d) to es-timate the discrete peak positions. We can estimate the carrier densities (n_{2D}) corresponding to each discrete peak at low tem-peratures (Figure S8) through

$$n_{2D} = \frac{(V_g - V_{th})C_g}{e} \quad (2)$$

where V_{th} is the threshold voltage, C_g is the gate capacitance den-sity, and e is the charge of a single electron. Consequently, according to the equation

$$\Delta E_F = \frac{h^2 \times \Delta n_{2D}}{4\pi \times m^*} \quad (3)$$

the discrete energy levels can be calculated by converting the car-rier densities to the shift of the Fermi level (E_F) with occupied en-ergy states from the bottom of the MoS_2 conduction band [50]. We estimate the discrete energy levels E_N ¼ 2.03, 5.41, 11.25, and 21.54 meV for N ¼ 1, 2, 3, and 4, corresponding to the oscillation peaks (Fig. 3d). For an ideal infinite potential well, the confinement energy levels (E_N) follow a quadratic relationship as

$$E_N = \frac{N^2 h^2}{8m^* L^2} \quad (4)$$

where N is the confined state number and L is the well width [51]. Assuming L ¼ 16 nm, the ideal discrete energy levels will be $E_{N\text{-infinite}}$ ¼ 2.6, 10.4, 23.4, and 41.6 meV for N ¼ 1, 2, 3, and 4, respectively. However, in our MoS_2 device, with Au contact, the barrier potential is determined by the Schottky barrier height (approximately 36e24 meV at a V_g of 2e8 V), which can be calculated with the 2D thermionic emission model (Figure S9). Taking the graphical solution with the transcendental equation for a finite potential well [51,52], the discrete energy levels are esti-mated as $E_{N\text{-finite}}$ ¼ 1.91, 7.34, 15.6, and 23.7 meV (N ¼ 1, 2, 3, and 4, respectively), as shown in Fig. 3e. The small variation between the model of the finite potential well and our experimental data (Fig. 3f) is attributed to the thin barrier width in our devices.

Compared to conventional field effect transistors (FETs), which normally utilize with continuous bands, the quantum transistor of the 2D Schottky-barrier quantum well here operates with multiple discrete energy levels, which reveals the multi-states in the transfer curves. For classical logic device application, our devices can be applied for multi-valued logic beyond the binary logic of conven-tional FETs. The similar concept was demonstrated in previous re-ports [53,54]. For quantum device application, our devices contain several discrete energy levels, which can be used for the quantum-well-based device application such as resonant tunneling transis-tors [31,32]. Moreover, the multiple discrete states with strong spin-orbit coupling in TMDCs would provide chances to create qubits for quantum computation application [55]. We note that the large-scale fabrication of our devices is feasible, as demonstrated in the previous report [40]. However, for practical application, the maximum observation temperature of the quantized states should be further increased, which is mainly determined by the quantum well width (the nanochannel length in our devices) and the effec-tive mass of channel materials. Further reducing the channel length is required. Moreover, the barrier height, which is defined by the Schottky barrier height between the contact metal and the channel

semiconductor, also influences the observation of the quantum effect. It should be large enough to confine the discrete states at the maximum observation temperature. (See another MoS_2 device with the channel length of approximately 12 nm in Figure S10 for more discussion.**)**

4.4. DIAMOND-LIKE PATTERNS

To comprehensively verify the quantum well characteristics, the maps for the corresponding G_m and G_m/V_{ds} with V_g and V_{ds} at 14 K are shown in Fig. 4a and b (See Figure S11 for the raw $G_m eV_g$ and $dG/dV_g eV_g$ curves with different V_{ds}). Certain diamond-like pat-terns are distinctly observed at low temperature, as illustrated by the dashed white lines. The diamond-like patterns smear out with increasing temperature. Further diamond-like pattern maps of G_m/ V_{ds} at different temperatures (see Fig. 4c and d and Figure S12) verify again the highest observation temperature of approximately 100 K. It should also be noted that such diamond-like patterns are normally observed in either quantum dots (quantization of energy states due to the con finement effect) or classical Coulomb blockade system (caused by charging effect, called Coulomb diamonds). In the classical Coulomb blockade system, uniformly discrete energy levels are formed from the charging energy. As a result, the Coulomb diamonds are uniform and symmetric [56]. In contrast,

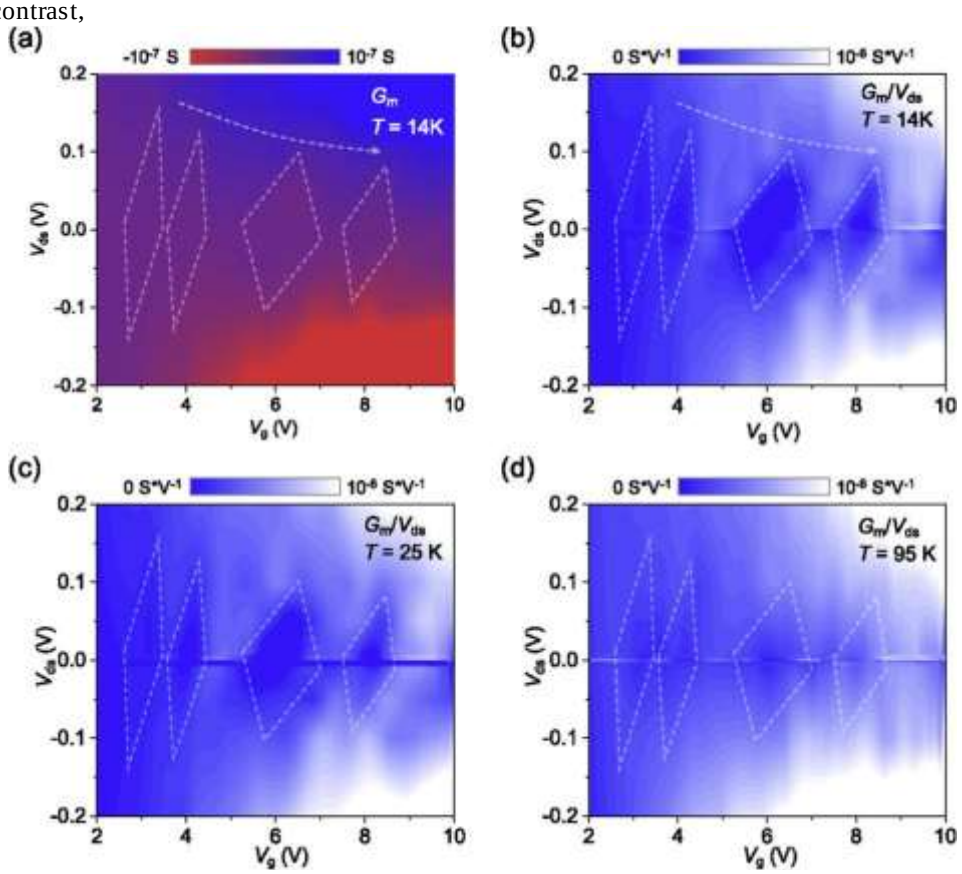

Fig. 4. Observation of diamond-like patterns. (a) G_m mapping with V_g and V_{ds} at 14 K. (bed) G_m/V_{ds} mapping at 14, 25, and 95 K.

our diamond-like pattern features are not uniform, which again informs the discrete energy levels inherently from the quantum confinement effect. Moreover, in the Schottky-barrier quantum wells, both the MoS_2 nanochannel and the Schottky barriers are tuned by V_g, modulating the height of the diamond-like patterns with V_g. The bias drop of V_{ds} is shared by both the MoS_2 nano-channel and the Schottky barriers, which is also different to clas-sical Coulomb blockade system with large solid barriers.

5. CONCLUSIONS. In conclusion, we observed the resonant tunneling and quan-tum oscillations up to 100 K in the Schottky-barrier quantum well of nanotransistors for 2D semiconductors with the channel length of approximately 16 nm. Our analysis indicates that the quantum confinement effect is dominant and contributes significantly to the formation of discrete energy levels in such a Schottky-barrier quantum well system, manifesting the oscillation features in the electrical characteristics in a simple vertical transistor with a MoS_2 channel without involving complex heterostructures. Our work sheds light on a deeper understanding of the transport character-istics in 2D semiconductor nanotransistors and provides a platform to investigate nanoscale quantum devices.

REFERENCES

[1] S.B. Desai, S.R. Madhvapathy, A.B. Sachid, J.P. Llinas, Q. Wang, G.H. Ahn, G. Pitner, M.J. Kim, J. Bokor, C. Hu, H.-S.P. Wong, A. Javey, MoS_2 transistors with 1-nanometer gate lengths, Science 354 (2016) 99e102, https://doi.org/ 10.1126/science.aah4698.

[2] M. Chhowalla, D. Jena, H. Zhang, Two-dimensional semiconductors for tran-sistors, Nat. Rev. Mater. 1 (2016) 16052, https://doi.org/10.1038/ natrevmats.2016.52.

[3] K. Kang, K.-H. Lee, Y. Han, H. Gao, S. Xie, D.A. Muller, J. Park, Layer-by-layer assembly of two-dimensional materials into wafer-scale heterostructures, Nature 550 (2017) 229e233, https://doi.org/10.1038/nature23905.

[4] K. Kang, S. Xie, L. Huang, Y. Han, P.Y. Huang, K.F. Mak, C.-J. Kim, D. Muller, J. Park, High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity, Nature 520 (2015) 656e660, https://doi.org/10.1038/ nature14417.

[5] Z. Lin, Y. Liu, U. Halim, M. Ding, Y. Liu, Y. Wang, C. Jia, P. Chen, X. Duan, C. Wang, F. Song, M. Li, C. Wan, Y. Huang, X. Duan, Solution-processable 2D semiconductors for high-performance large-area electronics, Nature 562 (2018) 254e258, https://doi.org/10.1038/s41586-018-0574-4.

[6] W. Cao, J. Kang, D. Sarkar, W. Liu, K. Banerjee, 2D semiconductor FETsdpro-jections and design for sub-10 nm VLSI, IEEE Trans. Electron Dev. 62 (2015) 3459e3469, https://doi.org/10.1109/ted.2015.2443039.

[7] X. Li, L. Yang, M. Si, S. Li, M. Huang, P. Ye, Y. Wu, Performance potential and limit of MoS_2 transistors, Adv. Mater. 27 (2015) 1547e1552, https://doi.org/ 10.1002/adma.201405068.

[8] Z. Ni, M. Ye, J. Ma, Y. Wang, R. Quhe, J. Zheng, L. Dai, D. Yu, J. Shi, J. Yang, Performance upper limit of sub-10 nm monolayer MoS_2 transistors, Adv. Electron Mater. 2 (2016) 1600191, https://doi.org/10.1002/aelm.201600191.

[9] J.P. Colinge, Multi-gate SOI MOSFETs, Microelectron. Eng. 84 (2007) 2071e2076, https://doi.org/10.1016/j.mee.2007.04.038.

[10] G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S.K. Banerjee, L. Colombo, Electronics based on two-dimensional materials, Nat. Nanotechnol. 9 (2014) 768e779, https://doi.org/10.1038/ nnano.2014.207.

[11] M. Chen, C. Lin, K.-H. Li, L.-J. Li, C.-H. Chen, C.-H. Chuang, M.-D. Lee, Y.-J. Chen, Y.-F. Hou, C.-H. Lin, C.-C. Chen, B.-W. Wu, C.-S. Wu, I. Yang, Y.-J. Lee, W.-K. Yeh, T. Wang, F.-L. Yang, C. Hu, Hybrid Si/TMD 2D electronic double channels fabricated using solid CVD few-layer-MoS_2 stacking for Vth matching and CMOS-compatible 3DFETs, IEEE Int. Electron Devices Meet (2014), https:// doi.org/10.1109/iedm.2014.7047163, 33.35.31-33.35.34.

[12] J. Miao, S. Zhang, L. Cai, M. Scherr, C. Wang, Ultrashort channel length black phosphorus field-effect transistors, ACS Nano 9 (2015) 9236e9243, https:// doi.org/10.1021/acsnano.5b04036.

[13] C.D. English, K.K. Smithe, R.L. Xu, E. Pop, Approaching ballistic transport in monolayer MoS_2 transistors with self-aligned 10 nm top gates, IEEE Int. Electron Devices Meet (2016), https://doi.org/10.1109/iedm.2016.7838355, 5.6.1-5.6.4.

[14] Y. Liu, J. Guo, Y. Wu, E. Zhu, N.O. Weiss, Q. He, H. Wu, H.-C. Cheng, Y. Xu, I. Shakir, Y. Huang, X. Duan, Pushing the performance limit of sub-100 nm molybdenum disulfide transistors, Nano Lett. 16 (2016) 6337e6342, https:// doi.org/10.1021/acs.nanolett.6b02713.

[15] A. Nourbakhsh, A. Zubair, R.N. Sajjad, A. Tavakkoli Kg, W. Chen, S. Fang, X. Ling, J. Kong, M.S. Dresselhaus, E. Kaxiras, K.K. Berggren, D. Antoniadis, T. Palacios, MoS_2 field-effect transistor with sub-10 nm channel length, Nano Lett. 16 (2016) 7798e7806, https://doi.org/10.1021/acs.nanolett.6b03999.

[16] L. Xie, M. Liao, S. Wang, H. Yu, L. Du, J. Tang, J. Zhao, J. Zhang, P. Chen, X. Lu, G. Wang, G. Xie, R. Yang, D. Shi, G. Zhang, Graphene-contacted ultrashort channel monolayer MoS_2 transistors, Adv. Mater. 29 (2017): 1702522, https:// doi.org/10.1002/adma.201702522.

[17] K. Xu, D. Chen, F. Yang, Z. Wang, L. Yin, F. Wang, R. Cheng, K. Liu, J. Xiong, Q. Liu, J. He, Sub-10 nm nanopattern architecture for 2D material field-effect transistors, Nano Lett. 17 (2017) 1065e1070, https://doi.org/10.1021/ acs.nanolett.6b04576.

[18] Z. Yang, X. Liu, X. Zou, J. Wang, C. Ma, C. Jiang, J.C. Ho, C. Pan, X. Xiao, J. Xiong, L. Liao, Performance limits of the self-aligned nanowire top-gated MoS_2 transistors, Adv. Funct. Mater. 27 (2017): 1602250, https://doi.org/10.1002/ adfm.201602250.

[19] X. Li, Z. Yu, X. Xiong, T. Li, T. Gao, R. Wang, R. Huang, Y. Wu, High-speed black phosphorus field-effect transistors approaching ballistic limit, Sci. Adv. 5 (2019): eaau3194, https://doi.org/10.1126/sciadv.aau3194.

[20] M. Reed, J. Randall, R. Aggarwal, R. Matyi, T. Moore, A. Wetsel, Observation of discrete electronic states in a zero-dimensional semiconductor nanostructure, Phys. Rev. Lett. 60 (1988) 535e537, https://doi.org/10.1103/ physrevlett.60.535.

[21] D. Ralph, C. Black, M. Tinkham, Spectroscopic measurements of discrete electronic states in single metal particles, Phys. Rev. Lett. 74 (1995) 3241e3244, https://doi.org/10.1103/physrevlett.74.3241.

[22] D. Ralph, C. Black, M. Tinkham, Gate-voltage studies of discrete electronic states in aluminum nanoparticles, Phys. Rev. Lett. 78 (1997) 4087e4090, https://doi.org/10.1103/physrevlett.78.4087.