International Journal of Engineering and Information Systems (IJEAIS)
ISSN: 2643-640X
Vol. 6 Issue 12, December - 2022, Pages: 50-56

VGA Monitor Interfacing

Rishabh Upadhyay

Student, Dept. of Electronics and Communication Engineering,
School of Studies in engineering and Technology, Guru Ghasidas Vishwavidyalaya, Bilaspur(C.G.)
Email - rishabhgmr97@gmail.com

Abstract— *VGA is a video transmission standard widely used in the display area. In the development of embedded systems, conventional microprocessors cannot achieve the timing of his VGA interface. This paper presents the efficient way of studying VGA system timing and connecting it to the hardware using the Nexys -4 DDR FPGA to display various colour patterns using the Xilinx Vivado software.*

Keywords— VGA, FPGA, Design, Verilog, Interfacing

1. INTRODUCTION

Almost all displays today are digital, whether it's a simple system displaying relatively static alphanumeric characters or a complex graphics system displaying rapidly changing image or video data. A digital display breaks down an image into small "picture elements" or pixels, each of which controls a small portion of the display. If the pixels are bright enough and small enough, the human eye can't see them individually, resulting in a smooth, continuous, and lifelike image. The larger the pixels, the more "pixelated" or jagged edges and contours become noticeable, reducing the perceived image quality. In fact, pixels occupying less than 1/30 her of about 30 of the human visual field cannot be perceived individually. To create the impression of smooth, fluid motion, pixels must update (or update) faster than the human eye can respond. In practice, no flicker or motion artifacts are perceptible if pixels are updated at 60Hz or higher for him [1].

The collection of pixels displayed on a particular monitor/display is called a "frame". It's easier to build a system that constantly updates all pixels in a frame, rather than trying to update only those pixels that have changed. A typical refresh controller sends 60 data frames to the display per second. This requires a continuous high-bandwidth data stream, even at moderate resolution. For example, consider an old 640 x 480 pixel VGA display. Since each of the 300,000+ pixels is defined by a byte of data that defines brightness and color, approximately 20MB of data must be transferred to the display per second. For a 1080P display with 16-bit pixel data, you need to send 1920 x 1080 x 2 x 60 = 248 MB/s to the display.

Now consider a picture displayed on a VGA display using 8-bit pixel data. The photo data requires 640 x 480 = 307K bytes and each byte he has to send to the display every 16ms (1/60Hz = 16ms). When using the processor to move data, each byte must be read from memory and each byte must be written to the video port. Each memory read requires at least 3 CPU clock cycles, and each video port write requires an additional 3 CPU clock cycles. Also, the address of each byte must be calculated (by incrementing the address inside the loop), which requires at least a load instruction, a store instruction, a comparison with the loop value, an increment instruction, and a branch. order. Each of these instructions also has to be fetched, so it can conservatively take another 12-14 CPU clock cycles. Considering all the operations required, moving 1 byte from memory to the display takes at least 20 CPU clock cycles, so moving 20 MB per second requires 400 million CPU cycles per second. increase. This exceeds the bandwidth many CPUs can support and is a significant fraction of a CPU's bandwidth. This is for repairing older, lower resolution displays. The more common 1080P displays require more than 4G cycles per second, and current generation processors can't run that fast. Of course, the CPU cannot support the necessary data movement requirements. Instead, special dedicated video controller circuitry is required.

1.1 VGA Port

The Nexys4 DDR board uses 14 FPGA signals to create one 4-bit VGA port per color and two standard sync signals (HS - Horizontal Sync and VS - Vertical Sync). The chroma signal uses a resistive divider circuit that works in conjunction with the VGA display's 75 ohm terminator to create 16 signal levels for each of the red, green, and blue VGA signals. This circuit, shown in Figure 11, produces a color video signal that smoothly varies between 0V (fully off) and 0.7V (fully on). This circuit can display 4096 different colors, one for each unique 12-bit pattern. The video controller circuit must be built into the FPGA to drive the sync and color signals at the appropriate times to create a working display system [6].

International Journal of Engineering and Information Systems (IJEAIS)
ISSN: 2643-640X
Vol. 6 Issue 12, December - 2022, Pages: 50-56

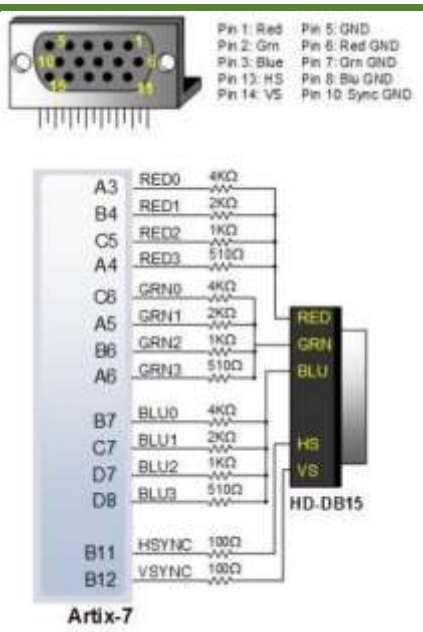


Figure 1: VGA interface [6]

1.2 VGA System Timing

Timing data for VGA systems is provided as associate degree example of however a VGA monitor behaves in 640 x 480 mode. CRT-based VGA displays use associate degree amplitude-modulated moving non particulate radiation (or cathode ray) to show data on a phosphor-coated screen. liquid crystal display displays use a series of switches which will apply a voltage to atiny low quantity of liquid to alter the permittivity of sunshine passing through the liquid on a pixel-by-pixel basis. the subsequent discussion is particular to gas-discharge tube displays, however liquid crystal display displays have evolved to use an equivalent signal timings as gas-discharge tube displays (so the "signals" discussion below applies to each CRTs and LCDs. gain). Color gas-discharge tube displays use 3 lepton beams (one for red, one for blue, and one for green) to excite phosphors that coat the inside of the show aspect of the ray tube. should be a Cymru font. kind three fonts cannot be used. alternative fonts will be used for special functions if desired..

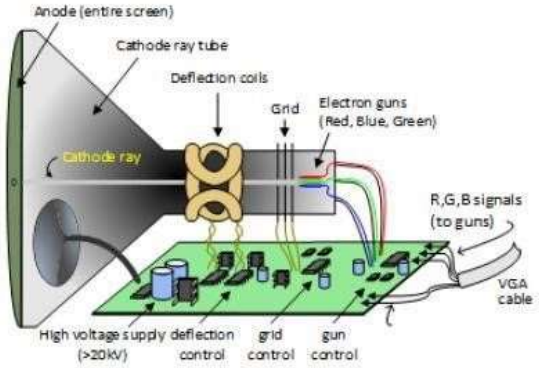


Figure 2: Colour CRT Display [6]

The nonparticulate radiation is emitted from associate degree "electron gun". associate degree electrode could be a heated, tapered cathode placed in shut proximity to a charged ringed plate referred to as a "grid". An electrostatic force applied through the grid pulls the beam of excited electrons far from the cathode. These bars ar driven by current flowing through the cathode. These particle beams ar ab initio accelerated toward the grid, however shortly expertise a far larger electrostatic force impact by charging the whole phosphor-coated show surface of the gas-discharge tube to 20 potential unit (or more). receive. receive. because the beam passes through the middle of the grid, it is focused into a slender beam that accelerates and hits the phosphor-coated show surface. The phosphor surface glows brilliantly at the purpose of impact and continues to glow for many microseconds when the beam is removed. the upper the present provided to the cathode, the brighter the phosphor can glow. Between the grille and therefore the screen surface the beam passes through the neck of the gas-discharge tube

Here, 2 coils of wire generate orthogonal magnetism fields. as a result of cathode rays are created from charged particles (electrons), they will be deflected by these magnetic fields. A current wave form is suffered the coil and interacts with the cathode rays, creating a magnetic flux across the show surface during a "grid" pattern horizontally from left to right and vertically from prime to bottom. gain. because the cathode rays move across the surface of the show, the present sent to the electrode will be raised or shriveled to change the brightness of the show at the purpose of impact of the cathode rays..

Information is simply displayed once the beam is taking possession the "forward" direction (left to right, prime to bottom), not once the beam returns to the left or prime of the screen. a lot of of the possible show time is so lost within the 'blanking' amount throughout that the beam is reset and stabilised to initiate a replacement horizontal or vertical show sweep. the scale of the beam, the frequency at that the beam will be copied on the show, and therefore the frequency at which the nonparticulate radiation will be modulated verify the resolution of the show.

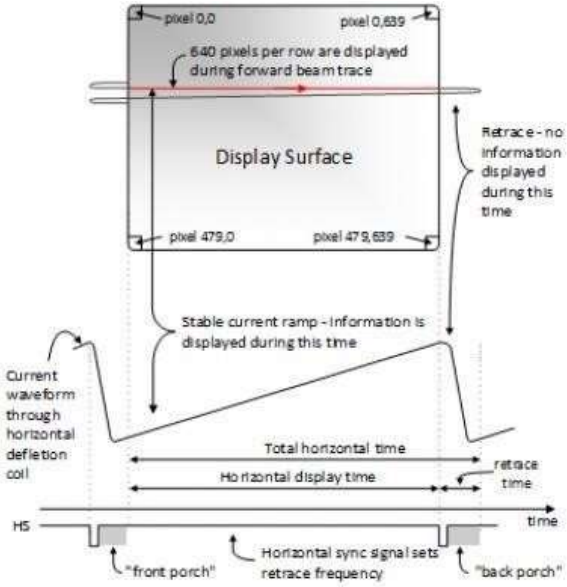
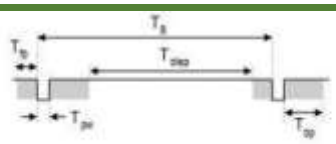


Figure 3: VGA Horizontal synchronization [6]

Modern VGA displays support totally different resolutions, and therefore the VGA feedback circuit determines the resolution by generating a clock signal to manage the formation pattern. one The controller must generate a three.3V (or 5V) correct pulse to line the frequency at that the deflection coil is energized in order that the video information is applied to the electrode at the proper time. A raster video display defines variety of "rows" cherish the amount of horizontal passes the cathode makes across the show space, and variety of "columns" cherish the area of every row within which a "pixel" is allotted. ' or pixels. Typical displays use 240-1200 rows and 320-1600 columns. the size of the show and therefore the range of rows and columns verify the scale of every component.

Video information is generally taken from video update memory. One or additional bytes are allotted for each component location (Nexys4 DDR uses twelve bits per pixel). The controller should index the video memory because the beam moves across the show and capture and apply video information to the show at the precise moment the non-particulate radiation crosses a selected component. The VGA controller circuit should generate the HS and VS temporal arrangement signals and coordinate the delivery of video information supported the component clock. A component clock defines the number of your time on the market to display one component of knowledge. The VS signal defines however typically the show is "refreshed", or however typically all the data on the show is redrawn. The minimum refresh rate could be a function of the display's phosphors and non-particulate radiation intensity, and sensible refresh rates range from fifty Hz to a hundred and twenty Hz. the amount of rows displayed at a selected refresh rate defines the horizontal "refresh" rate.



Symbol	Parameter	Vertical Sync			Horiz. Sync	
		Time	Clocks	Lines	Time	Clks
T_S	Sync pulse	16.7ms	416,800	521	32 us	800
T_{disp}	Display time	15.36ms	384,000	480	25.6 us	640
T_{pw}	Pulse width	64 us	1,600	2	3.84 us	96
T_{fp}	Front porch	320 us	8,000	10	640 ns	16
T_{bp}	Back porch	928 us	23,200	29	1.92 us	48

Figure 4: Signal timings of a 640-pixel by 480 row display using a 25MHz pixel clock and 60Hz vertical refresh [2]

The VGA feedback circuit decodes the output of the horizontal correct counter driven by the pixel clock to come up with the temporal arrangement of the HS signal. This counter will be accustomed establish each component location during a specific row. Similarly, the output of a vertical correct counter that increments on every HS pulse will be accustomed generate the temporal arrangement of the VS signal, which can be accustomed find a selected line. These 2 unceasingly running counters will be used to kind video RAM addresses. Since the temporal arrangement relationship between the beginning of the HS pulse and therefore the begin of the VS pulse isn't nominal, you'll be able to merely place a counter to form the video RAM address or minimize the decipher logic for correct pulse generation. increase.

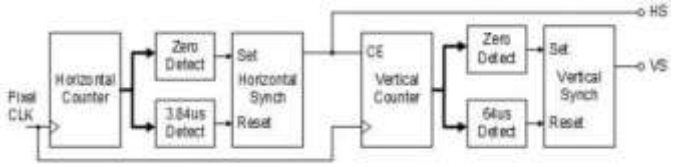


Figure 5: VGA Display controller block diagram

2. UNDERSTANDING THE INTERFACING DETAILS WITH FPGA

The Nexys 4 DDR FPGA board used in this project has an onboard VGA connector and has five active signals such as horizontal sync, vertical sync, and video signals (red, green, blue). The video signal for VGA is an analog signal, so common video controllers use D-A. With the availability of a three-colour video signal, eight different colours can be displayed on the screen. To do this, you must assign the correct binary input combination to the VGA connector. The following table shows the various possible colour combinations. [4]

Red (R)	Green (G)	Blue (B)	Resulting Colour
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

Table 1: Three bit VGA combinations

International Journal of Engineering and Information Systems (IJEAIS)
ISSN: 2643-640X
Vol. 6 Issue 12, December - 2022, Pages: 50-56

3. RESULT AND SIMULATION

3.1 Part 1

In this part of VGA display I have tried to display the 8 colours in vertical fashion using the 3-bit combinations of the 3 colour signals (red, blue and green) as shown above. The display size frame is of size 640*480 pixels, so to display vertically we have 8 columns of width 80 pixels and height 480 pixels each. The result obtained is thus shown below.

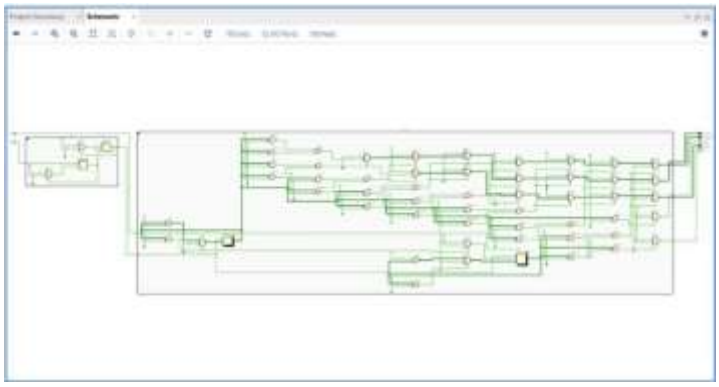


Figure 6: Schematic of Part 1

Figure 7: Monitor display of Part 1

3.2 Part 2

In this part of VGA display I have tried to display all the previously displayed vertical bars of 8 different colours in the top of the leftmost bar thus making the height of the bar 60 pixels (480 / 8 = 60) and the width of the bar at the same 80 pixels as of the vertical bar height while the remaining bars have been untouched. We can have 64 (80*60) pixel bars in the whole frame. The result obtained is thus shown below.

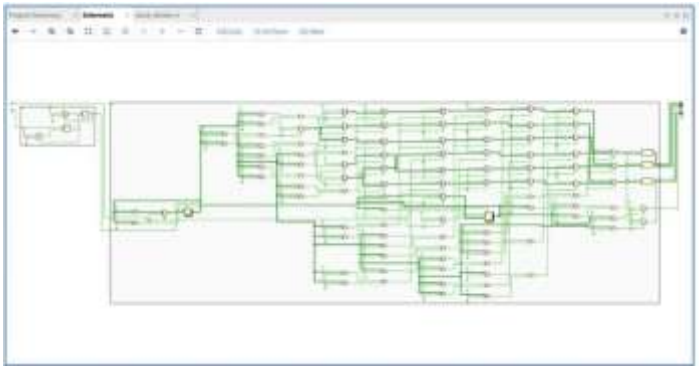


Figure 8: Schematic of Part 2

Figure 9: Monitor display of Part 2

4. CONCLUSION

FPGAs are electronic devices due to their many strong advantages and few (if any) drawbacks from an application point of view. For these reasons, it has become the digital processor of choice in many situations. By choosing an FPGA that matches our design, we can achieve high performance, low power consumption, and low cost. The VGA monitor interface system may also need more work to make the display sharper.

ACKNOWLEDGEMENT

I would like to express my sincere gratitude and thanks to my mentor during my summer internship at IIT BHU, Dr. Kishor P. Sarawadekar and my father Dr. Krishna Nand Upadhyay who always during writing of this paper.

DATA AVAILABILITY
Not Applicable

COMPETING INTERESTS
Not Applicable

FUNDING
Not Applicable

AUTHOR CONTRIBUTIONS

The work is the sole contribution of the author with help taken from his guide.

ETHICS APPROVAL

The study was carried out and approved by the guide at Indian Institute of Technology, BHU and the required data is not applicable.

REFERENCES

[1] https://digilent.com/reference/programmable-logic/nexys-4-ddr/start

[2] VGA Timing. Accessed march 7 2014 martin.hinner.info/vga/timing.html

[3] VGA Interface and Pin out. Accessed march 7 2014http://www.allpinouts.org/index.php/VGA_15_Pin

[4] RGB Color Model. Accessed march 7 2014 http://en.wikipedia.org/wiki/RGB_color_model

[5] VESA. Monitor Timing Specification Version 1.0 Rev. 0.8. Technical report, September 1998.

[6] Xilinx. Nexys-4 DDR FPGA: Technical report, September 2014.

[7] Xilinx. Vivado Design suite User Guide. October 2021

[8] Guohui Wang, Yong Guan, and Yan Zhang. Designing of VGA Character String Display Module Based on FPGA. In International Symposium on Intelligent Ubiquitous Computing and Education(IUCE), pages 499–502, 2009.

[9] Javier Valcarce Garcia. Monochrome Text-Mode VGA Video Display Adapter. Technical report, 2009. Van-Huan Tran and Xuan-Tu Tran. CoMoSy: a Flexible System-onChip for Embedded Applications. Journal for Research, Development and Application on Information and Communication Technology, 2, 2011.

Authors

Rishabh Upadhyay, Final year B.Tech student of Electronics & Communication Engineering at Guru Ghasidas Vishwavidyalaya, Bilaspur..